In the Specification:

Please replace the paragraph beginning on page 6 line 28 with the following amended paragraph:

Preferably, one QP context cache is provided for the requester communication flow handled by the HCA, and another is provided for the responder communication flow. Most preferably, each of these caches is used for both sending and receiving packets on the respective flow. In some preferred embodiments of the present invention, the HCA is configured to handle both of these flows using common hardware resources, rather than maintaining separate hardware paths for these functions as in devices known in the art. This novel HCA architecture is described in ~~another~~ U.S. patent application publication number 2002/0152327, entitled "Network Interface Adapter with Shared Data Send Resources," filed Dec. 4, 2001 which is assigned to the assignee of the present patent application, and whose disclosure is incorporated herein by reference.

Please replace the paragraph beginning on page 17 line 13 with the following amended paragraph:

Host 24 and HCA 22 are connected to a system memory 38 via a suitable memory controller 36, as is known in the art. The HCA and memory typically occupy certain ranges of physical addresses in a defined address space on a bus connected to the controller, such as a Peripheral Component Interface (PCI) bus. In addition to the host operating system, applications and other data (not shown), memory 38 holds data structures that are accessed and used by HCA 22. These data structures preferably

include QP context information 42 maintained by the HCA, and descriptors 44 corresponding to WQEs to be carried out by HCA 22. Certain aspects of the structure and use of QP context information 42 for controlling access to QPs by host processes are described in greater detail in **[[a]]** U.S. patent application publication number 2002/0165899 entitled "Multiple Queue Pair Access with a Single Doorbell," filed Nov. 26 , 2001. Descriptors 44 are preferably prepared and executed in the form of a linked list, as described in ~~another~~ U.S. patent application publication number 2001/0049755 entitled "DMA Doorbell," filed May 31, 2001. Both of these applications are assigned to the assignee of the present patent application, and their disclosures are incorporated herein by reference.

Please replace the paragraph beginning on page 18 line 4 with the following amended paragraph:

Fig. 2 is a block diagram that schematically shows details of HCA 22, in accordance with a preferred embodiment of the present invention. The blocks shown in the figure are primarily those that are involved in using and updating QP context information. For the sake of simplicity, elements of HCA 22 that are not essential to an understanding of the present invention are omitted. The blocks and links that must be added will be apparent to those skilled in the art. Further details of the HCA are described in the above-mentioned patent application entitled, "Network Interface Adapter with Shared Data Send Resources," as well as in ~~another~~ patent application publication number 2002/0150106 entitled, "Handling Multiple Network Transport Service Levels with Hardware and Software Arbitration," filed ~~on even date~~ January 23, 2002, whose disclosure is incorporated herein by reference.